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A pulse interrupt is a variant of an edge model. You must ensure that the pulse is sampled on the rising

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edge of the Cortex-M4 clock, FCLK, instead of being asynchronous. For level interrupts, if the signal is not deasserted before the return from the interrupt routine, the interrupt again enters the pending state and re-activates.

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Manual processor that features low gate count, low interrupt latency, and low-cost debug. The Cortex-M4F is a processor with the same capability as the Cortex-M4 processor, and includes floating point arithmetic functionality (see Chapter 7 Floating Point Unit).

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Both processors are intended for deeply embedded applications that require fast interrupt response features.

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M4 manual, as supplied by ARM. Device Refers to an implemented device, supplied by an ARM partner, that incorporates a Cortex-M4 processor. In particular, your device refers to the particular implementation of the Cortex-M4 that you are using.

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In this manual, in general: † any reference to the processor applies to either the Cortex-M4 processor or the Cortex-M4F processor, as appropriate † any reference to the

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Cortex-M4 processor applies also to the Cortex-M4F processor, as appropriate. The context makes it clear if information applies to only one of the processor options.

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