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~~Ignitions With Delays~~

It was both non-trivial and used the board's features nicely. But it has the message hard coded into the Verilog which means you need to rebuild the FPGA every time you want to change it.

~~How To Add UART To Your FPGA Projects~~

Some of the guidelines

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which designer needs to follow to make the design synthesizable are:

- Infer registers

Avoid combinational feedback loops •

Specify complete sensitivity list to avoid

...

~~Enforcing Design Rules to Develop Reusable IP~~

At this level, the channels are blocking

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pin-accurate ... This
kind of simulation may
be timed with delay
annotations and may use
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